

<p style="text-align: center;">O I P E INFORMATION DISCLOSURE STATEMENT BY APPLICANT <i>JUL 11 2006</i> <i>(use as many sheets as necessary)</i></p>				Complete if Known	
				Application Number	10/521,054
				Filing Date	January 12, 2005
				First Named Inventor	Takashi Yokokawa
				Art Unit	2133
				Examiner Name	RIZK, Samir Wadie
Sheet	1	of	1	Attorney Docket Number	09812.0200-00000

U.S. PATENTS AND PUBLISHED U.S. PATENT APPLICATIONS					
Examiner Initials	Cite No. ¹	Document Number	Issue or Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear
		Number-Kind Code ² (if known)			
		US-			

Note: Submission of copies of U.S. Patents and published U.S. Patent Applications is not required.

FOREIGN PATENT DOCUMENTS						
Examiner Initials	Cite No. ¹	Foreign Patent Document	Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear	Translation ⁶
		Country Code ³ Number ⁴ Kind Code ⁵ (if known)				

NON PATENT LITERATURE DOCUMENTS					
Examiner Initials	Cite No. ¹	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published.			Translation
SR		Robert G. Gallager, <i>Low-Density Parity Check Codes</i> (M. I. T. Press 1963).			
SR		David J. C. MacKay, "Good Error-Correcting Codes Based on Very Sparse Matrices," <i>IEEE Transactions on Information Theory</i> , vol. 45, no. 2, pp. 399-431, March 1999.			
SR		Michael G. Luby, Michael Mitzenmacher, M. Amin Shokrollahi & Daniel A. Spielman, "Analysis of Low Density Codes and Improved Design Using Irregular Graphs," <i>Proceedings of ACM Symposium on Theory of Computing</i> , pp. 249-58 (1998).			
SR		C. Howland & A. Blanksby, "Parallel Decoding Architectures for Low Density Parity Check Codes," <i>Symposium on Circuits and Systems</i> , part IV, pp. 742-45 (2001).			
SR		Engling Yeo, Payam Pakzad, Borivoje Nikolic & Venkat Anantharam, "VLSI Architectures for Iterative Decoders in Magnetic Recording Channels," <i>IEEE Transactions on Magnetics</i> , vol. 37, no. 2, pp. 748-55, March 2001.			

Examiner Signature	/Samir Rizk/ (09/28/2006)	Date Considered
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